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forming a semiconductor layer on a substrate;
forming a gate insulating film on said semiconductor layer;
forming a gate electrode above said gate insulating film and a gate line in electrical contact with said gate electrode;
forming a source region and a drain region in said semiconductor layer by adding impurities thereto as donors or acceptors using said gate electrode as a self alignment mask;
simultaneously forming an overlying gate insulator on a top and sidewalls of said gate electrode and said gate line by anodic oxidation of said gate electrode and said gate line to reduce the dimensions of said gate electrode and said gate line and simultaneously form a lateral offset, ΔL , from said source region and said drain region to the sidewalls of said gate electrode; and
forming a data line in electrical contact with said source region and crossing over said gate line at a cross-over location, wherein said overlying gate insulator is located between said data line and said gate line at said cross-over location to insulate said data line from said gate line.

24. The method of claim 23 wherein said gate electrode is comprised of tantalum, and wherein said overlying gate insulator comprises tantalum oxide.

25. The method of claim 23 wherein said gate electrode is selected from the group consisting of tantalum and aluminum.

26. The method of claim 23 wherein the semiconductor layer is a silicon layer formed by decomposing a silane gas using CVD.

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27. The method of claim 23 wherein the semiconductor layer is a polysilicon layer formed by first forming an amorphous silicon layer and annealing the amorphous silicon layer at a temperature within a range of 450° C. to 700° C. for 12 to 70 hours.

28. The method of claim 23 wherein the gate insulating film is sputter formed on a surface of the semiconductor layer.

29. The method of claim 23 wherein the source region and the drain region are formed by implanting phosphorous ions into the semiconductor layer through the gate insulating film.

30. The method of claim 29 wherein the implanted phosphorous ions are radiated with a laser to reduce the resistance level in the semiconductor layer.

31. The method as defined in claim 23 wherein the overlying gate insulator is formed having a lateral thickness, ΔI , which is greater than the lateral offset, ΔL .

32. The method as defined in claim 23 wherein the step of forming the overlying gate insulator by anodic oxidation decreases the width of the gate electrode by about twice the lateral offset, ΔL --

REMARKS

As discussed hereinafter, new claims 23-32 have been added to initiate an interference with U.S. Patent No. 5,561,075 ('075), the '075 patent being based on a Rule 60 divisional application of U.S. Patent No. 5,383,366 to Nakazawa wherein the claims of the '366 patent are device claims and those of the '075 patent are method claims.